

REV	Description	DATE	BY
A4A	Initial production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AMS359 were actually AMS352. This revision uses the correct parts.	1/2/2013	GC
A5A	<ol style="list-style-type: none"> Deleted R29-R44 from the LCD lines. Added 47pf capacitors C156-C173 to LCD data lines to ground. Changed schematic revision to A5A. Changed a few footprints after PCB update for above changes. Added access point for the battery function of the TPS65217C. Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin. Added power button to enable sleep, wakeup, power down and power up features on the system. Added Modification to add 100K ohm resistor to ground to prevent crosstalk when serial cable is not plugged in. 	2/8/2013	GC
A5B	<ol style="list-style-type: none"> Added 100K pull-down on J1 pin 4 to prevent crosstalk when serial cable is not connected into PCB layout. Changed the LED resistors to 4.75K to lower the brightness. 	5/21/2013	GC
A5C	<ol style="list-style-type: none"> Changed R46, R47, R48 to 0 ohms. Changed R45 to 22 Ohms. Change was made due to production failures on some boards due to differences in impedances.	6/12/2013	GC
A6	<ol style="list-style-type: none"> Moved the enable for the VDD_3V3B regulator to VDD_3V3A rail. Change was made to reduce the delay between the ramp up of the 3.3V rails. Added a AND gate to the SYS_RESETn circuitry. There is a small chance that on power up the nRESETOUT signal on the processor may go high, causing the SYS_RESETn signal to go HI before it should. This change reenforces the reset with the PORZn reset signal. Added optional zero ohm resistor to tie OSC_GND to system ground. 	7/25/2013	GC

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3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

NOTE: PCB Revision for this board is Rev B5.

This schematic is *NOT SUPPORTED* and DOES NOT constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss.

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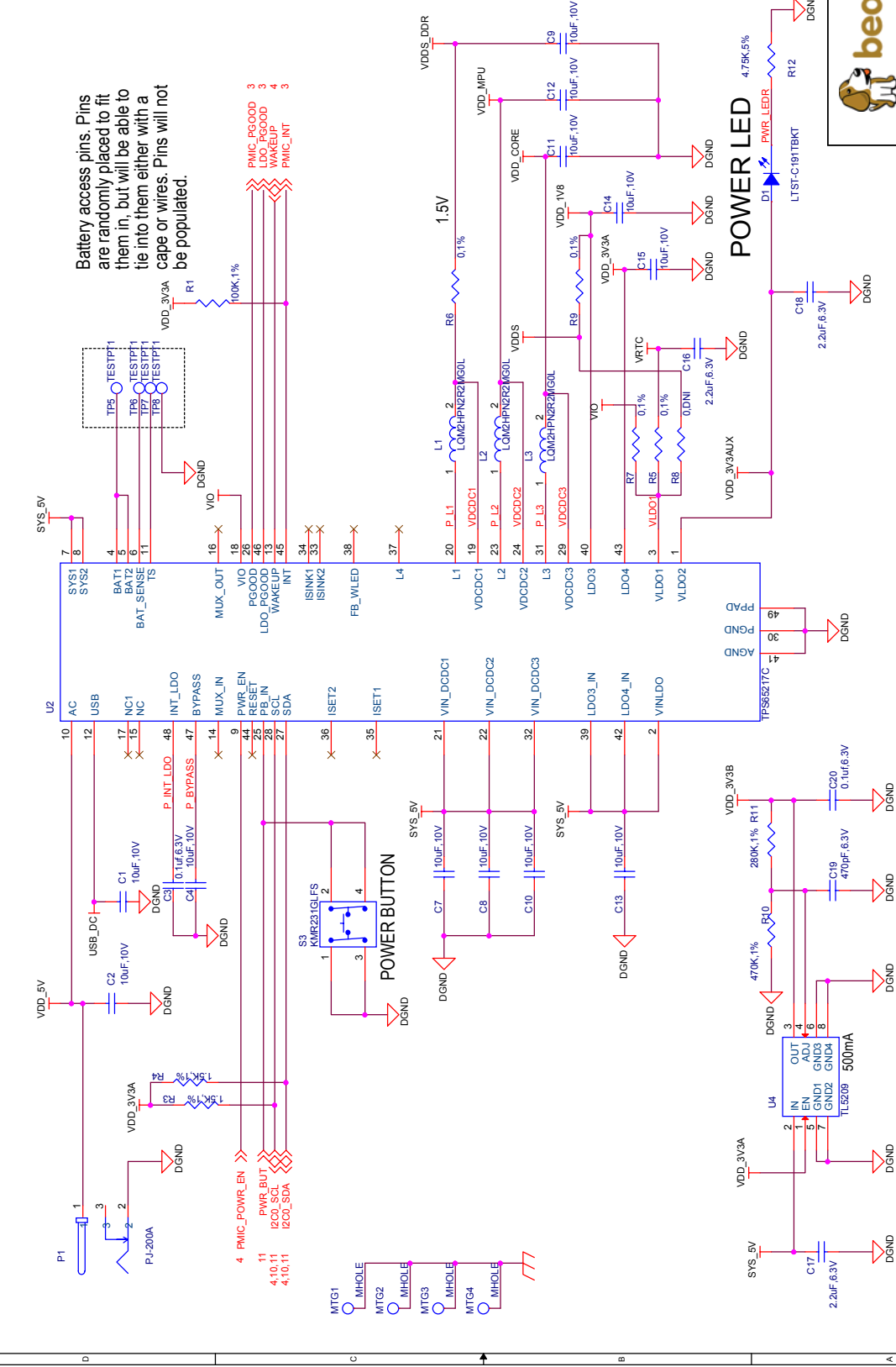
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TP1
TESTPT1
DGND

Battery access pins. Pins are randomly placed to fit them in, but will be able to tie into them either with a cape or wires. Pins will not be populated.

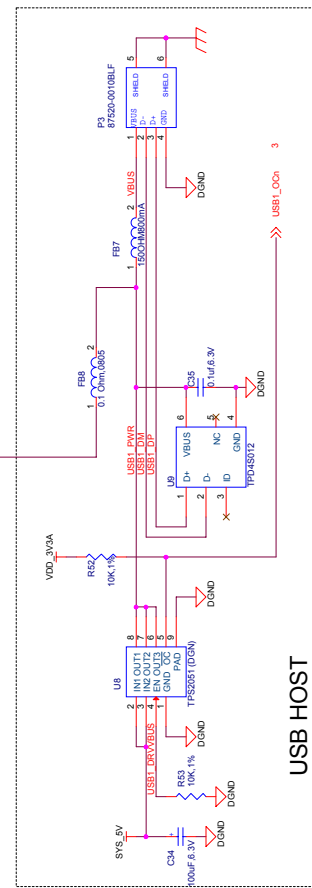
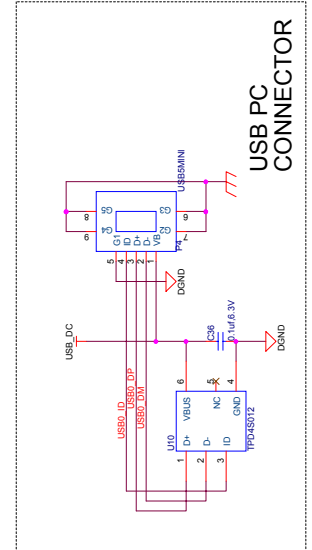
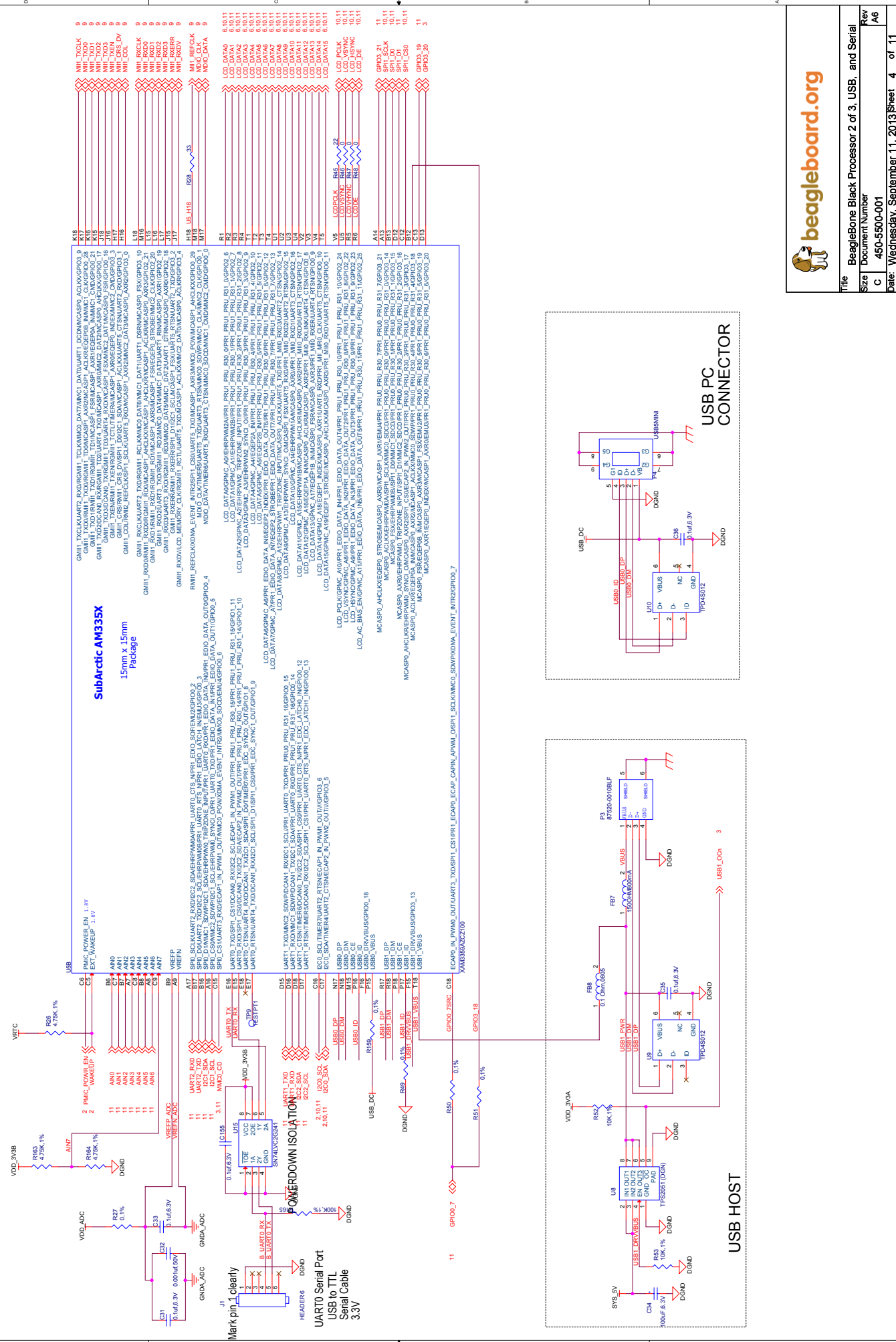


Title		BeagleBone Black Power Management	
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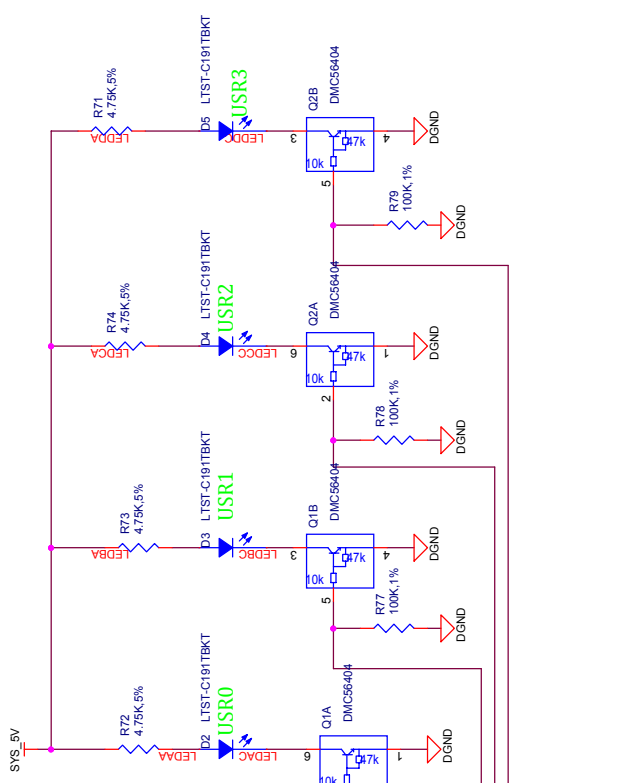
1 2 3 4 5

D C B A

SubArctic-AM335X
 15mm x 15mm
 Package



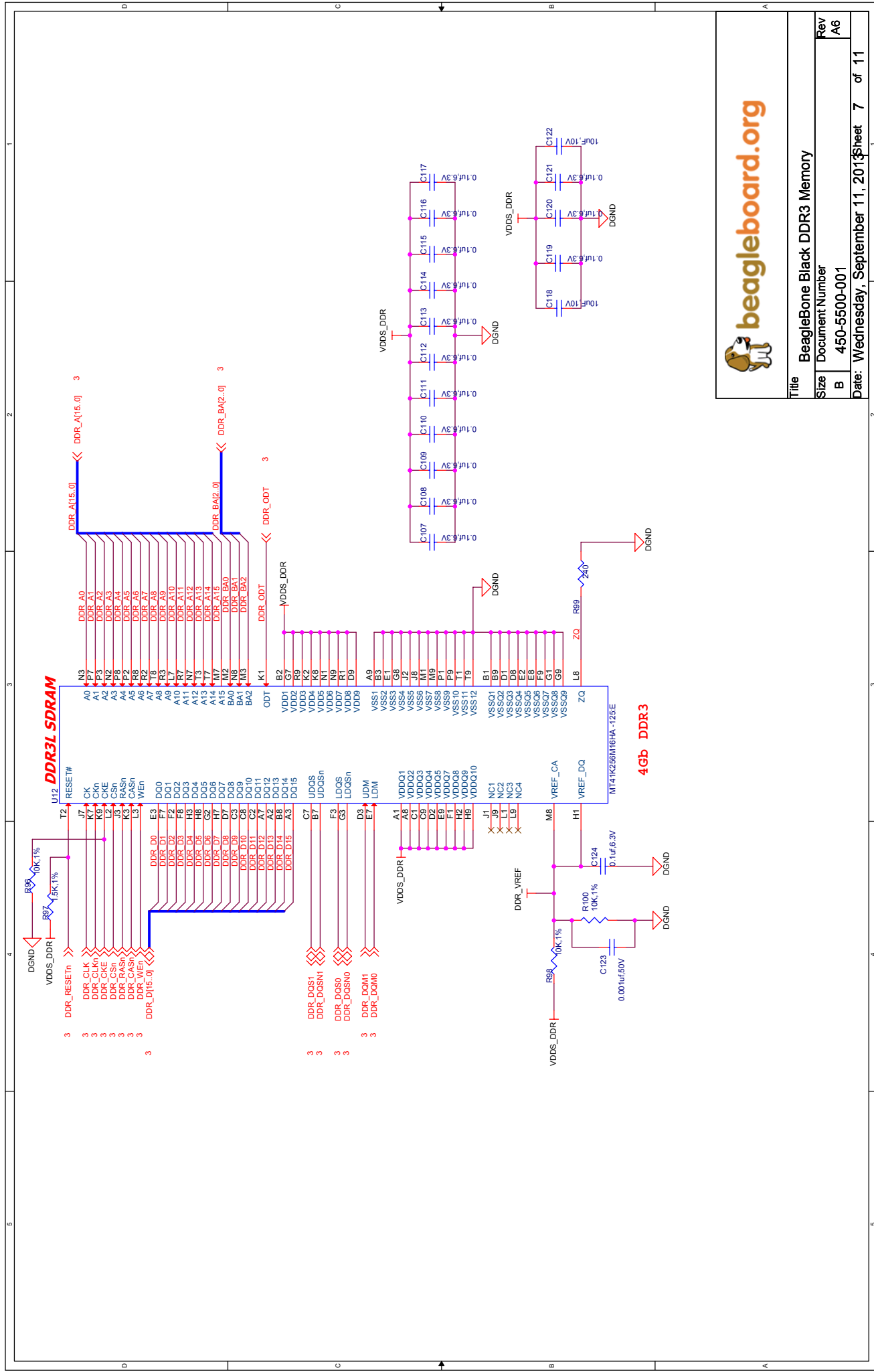
Mark pin 1 clearly
 USB to TTL
 Serial Cable
 3.3V



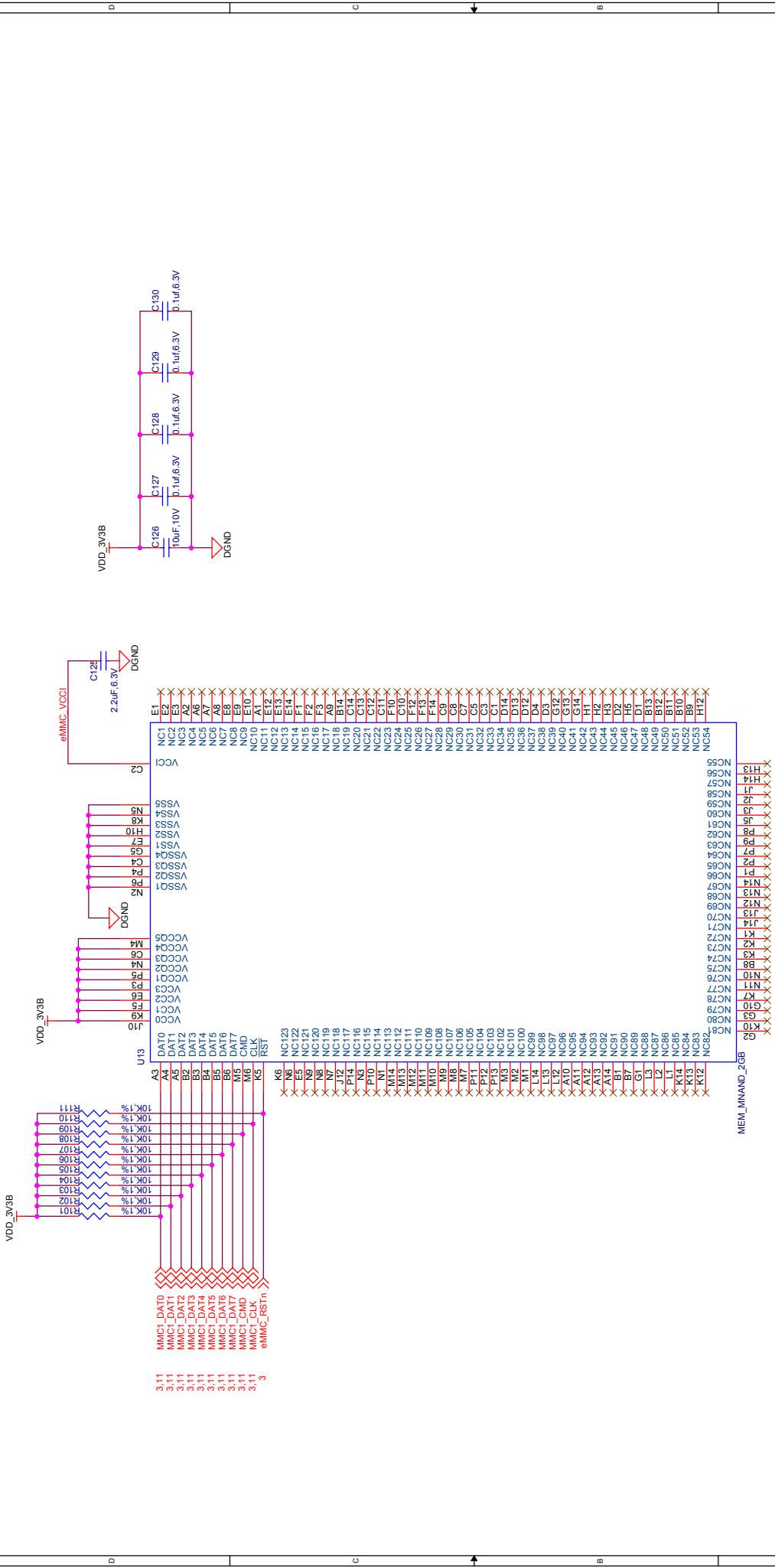
SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC0 UART0 USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	MMC0 USB0[5] UART0



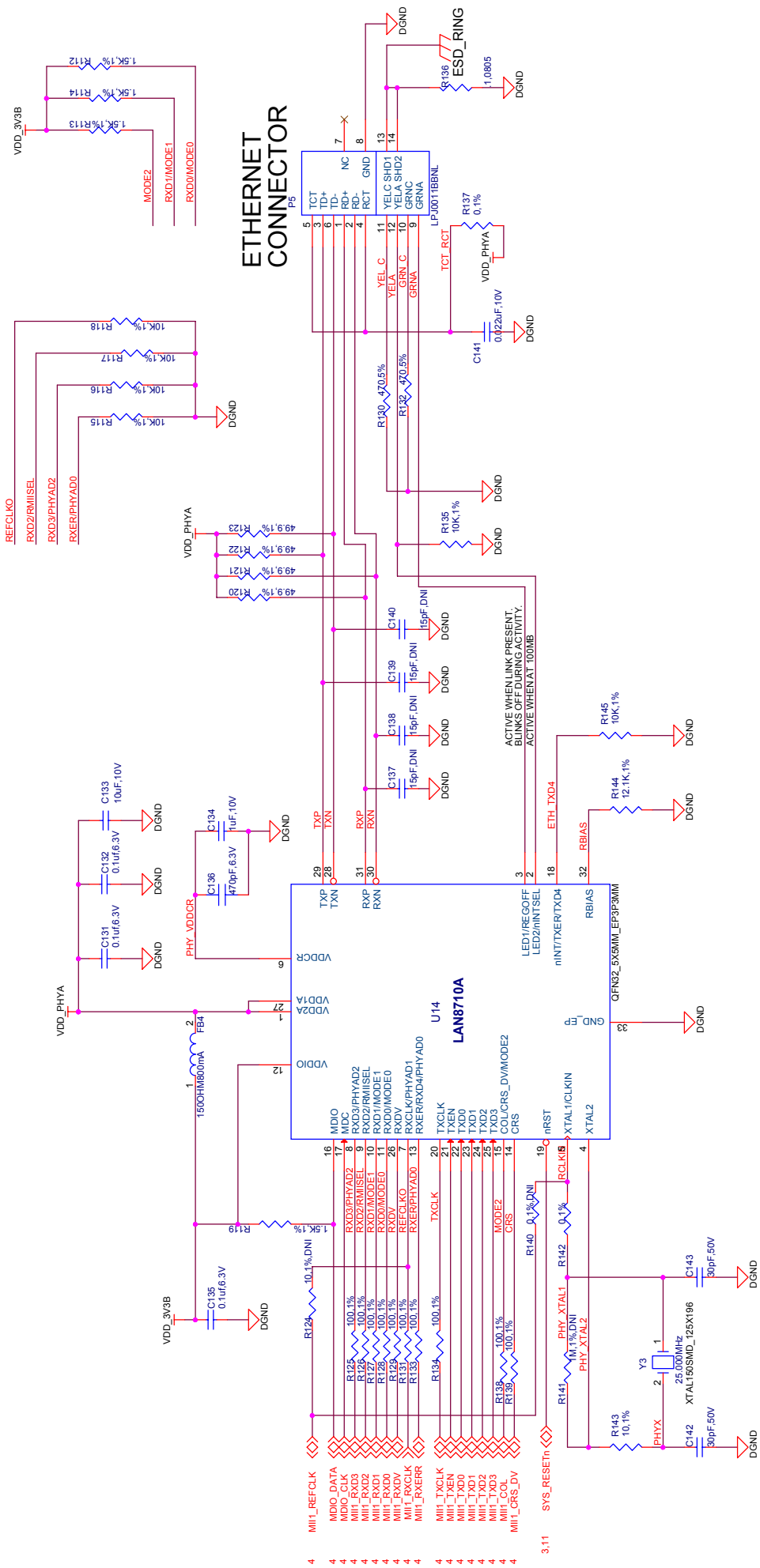
Title		BeagleBone Black LED, Configuration, and Reset
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Title		BeagleBone Black DDR3 Memory
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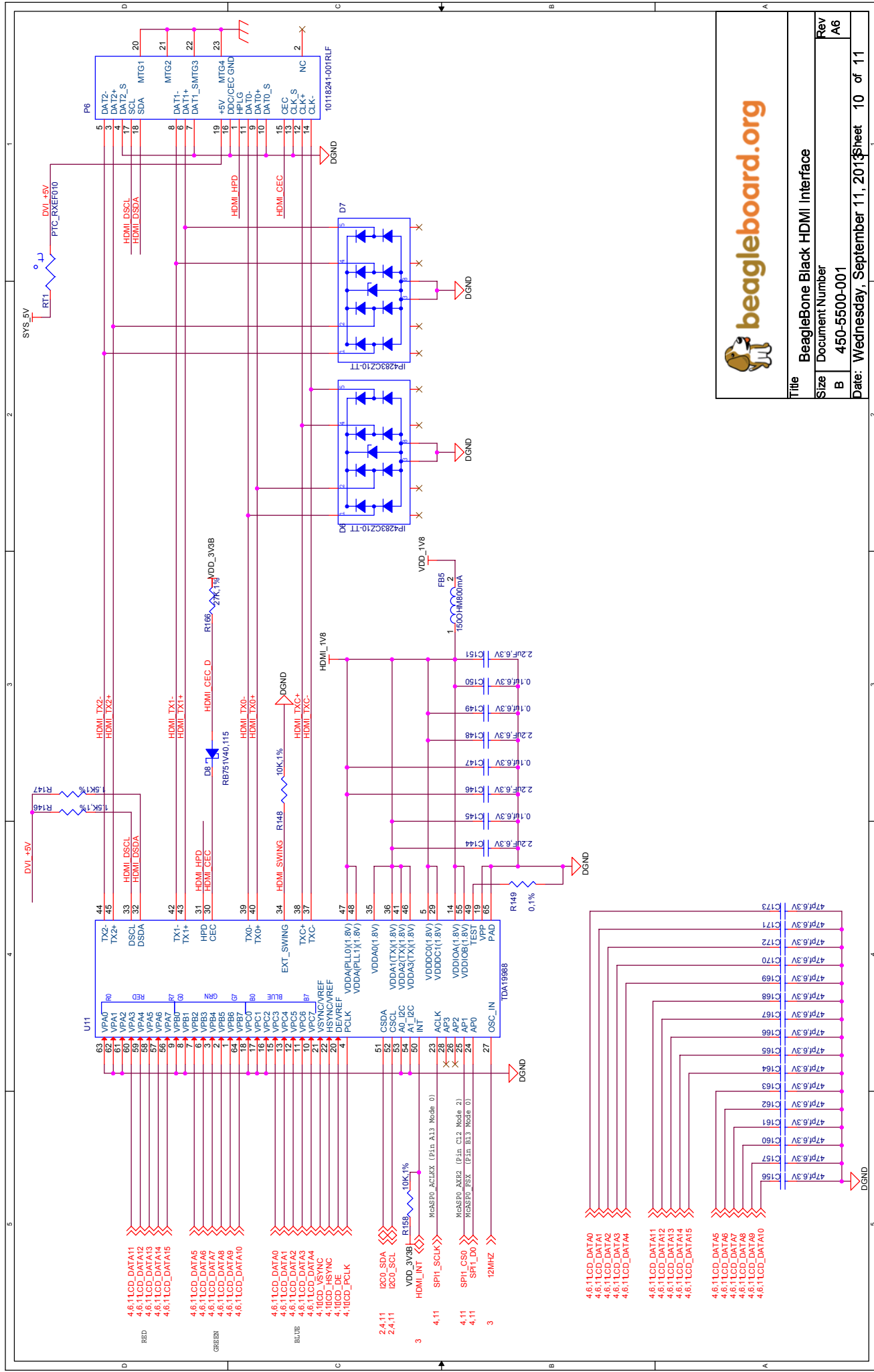


Title		Beagle BoneBlack 2G eMMC	
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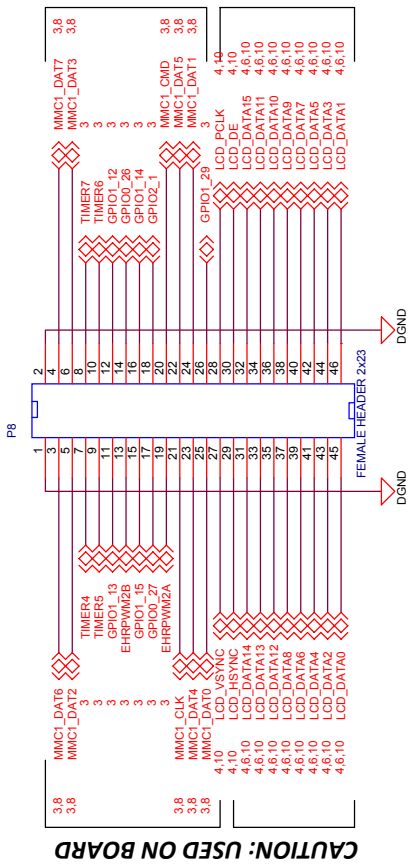
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Title		BeagleBone Black Ethernet	
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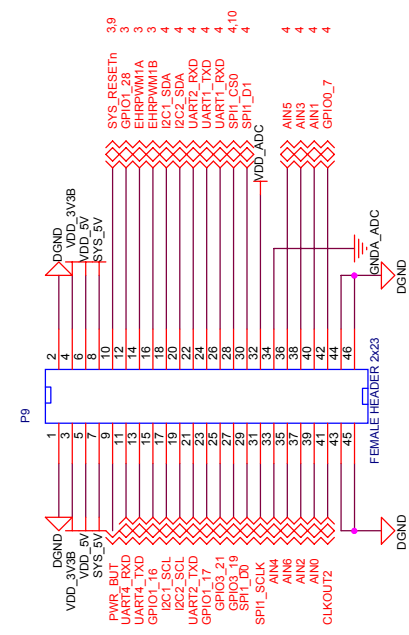


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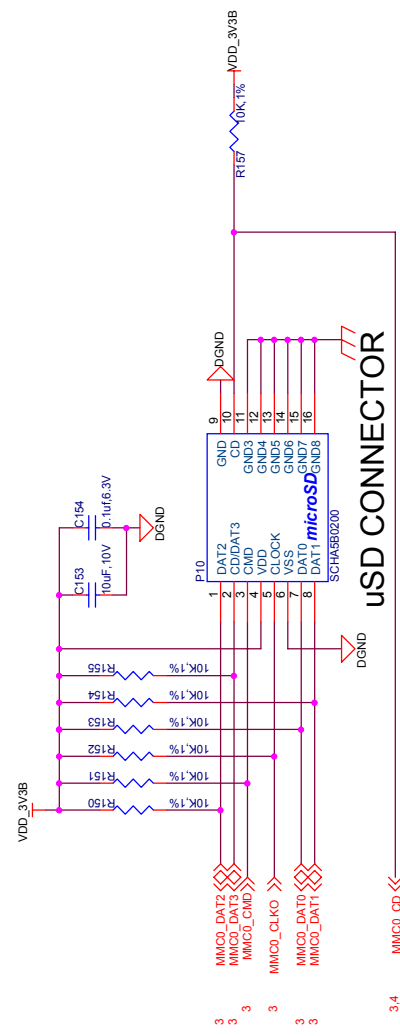
Title		BeagleBone Black HDMI Interface
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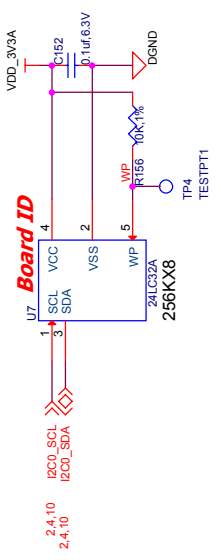
EXPANSION HEADER



EXPANSION HEADER



uSD CONNECTOR



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