Datasheet

VL805
4-Port USB 3.0 Host Controller

Sep. 4, 2014
Revision 0.93

VIA Labs, Inc.
www.via-labs.com
7F, 529-1, Zhongzheng Rd.,
Xindian District, New Taipei City 231 Taiwan
Tel: (886-2) 2218-1838
Fax: (886-2) 2218-8924
Email: sales@via-labs.com.tw

Revision History

Rev #	Status*	Date	Author	Reason for change/description
085		2012/11/13	John	1. Add china charging 2. Add In house UAS/Turbo driver 3. Add Compatible with Windows 8 inbox driver
086		2012/11/30	John	1. Add Linux driver support 2. Add Host Controller Capability Registers & Host Controller Runtime Registers 3. Add work temperature
087		2012/12/13	John	1. Refine the drawing of mechanical specification.
088		2013/03/18	John	1. Fix some typing errors
090		2013/05/27	John	1. Add triangle mark on VL806 pinout diagram.
091		2013/09/05	John.	1. Add the pin description for VCCA33SSM
092		2013/11/29	John	1. Modify the driver support
093		2014/9/4	John	1. Add Part Number for order information

Table of Contents

1. Product Features----4
2. VL805 System Overview ----5
3. VL805 Pin Diagram ----6
4. PIN Function ----7
5. Electrical Characteristics---- 9
6. PCI Configuration Registers ----11
7. Host Controller Capability Registers ---- 18
8. General Reflow Profile Guidelines ---- 23
9. Package Mechanical Specifications ---- 24
10. Package Top Side Marking ---- 26
11. Order Information ---- 26

1. Product Features

VL805
4-Port USB 3.0 Host Controller

- **Compliant to Universal Serial Bus 3.0 Specification Revision 1.0**
  - Supports all transfer types: Control, Bulk, Stream, Interrupt, Isochronous
- **Compliant to Universal Serial Bus 2.0 Specification**
- **Compliant to eXtensible Host Controller Interface (xHCI) Specification Revision 1.0**
  - Support USB debugging capability on all super-speed ports
- **Support Legacy USB Function**
  - Four down-stream ports support SuperSpeed(SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)
- **Support Battery Charging Specification**
  - Compliant to Battery Charging Specification Revision 1.2
  - Apple Charging
  - China Charging
- **Firmware Upgrade**
  - Support firmware upgrade with software tool under Microsoft DOS and Windows XP, Vista, Windows 7, Windows 8.
  - Option to integrate firmware in system BIOS (for on-board design.)
- **Compliant with PCI Express Base Specification 2.0**
  - Supports Express Card Standard
- **In-house USB and PCIe PHY employs advanced CMOS process to reduce power consumption**
  - 3.3 V and 1.05 V power supply
  - USB 3.0 low power states support
- **System Clock**
  - 25 MHz Crystal
- **Software**
  - Initial xHCI Host Controller Driver Support for Windows 8/8.1, Windows 7
    - Bulk Only Transfer (BOT)
    - USB Attached SCSI Protocol (UASP) mode

  - Provide In-House UAS/Turbo driver on Windows 7.
  - Compatible with Windows 8/8.1 in box driver.
  - Compatible with Linux xHCI driver since Linux kernel 3.2.53 and after.
- **Physical**
  - QFN 68 green package (8x8)
- **Applications**
  - Motherboard
  - Notebook/Netbook
  - Express Card
  - Add-in Card
  - Embedded System
  - Docking Station

2. VL805 System Overview

VLI VL805 is a single chip USB 3.0 Host controller which enables a PCI Express equipped platform to interface with USB Super-Speed (5 Gbps), High-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) devices. The root hub consists of two downstream facing ports, allowing simultaneous operation of up to 31 peripheral devices. The VL805 has an x1 PCI Express 2.0 bus interface that is backwards compatible with PCI Express 1.0.

The VL805 complies with the Universal Serial Bus 3.0 Specification and Intel's eXtensible Host Controller Interface (xHCI), and is fully backward compatible with USB 2.0 and 1.1 specifications, ensuring seamless connectivity of legacy USB devices.

With well-planned pinout and advanced process, VL805 based devices enjoy easy layout and low working temperature in a compact footprint. Sideband signal pins are available for showing power enable, over current, and LED status. VL805 is available in QFN 68 green package (8x8 mm) to fit small form-factor designs.

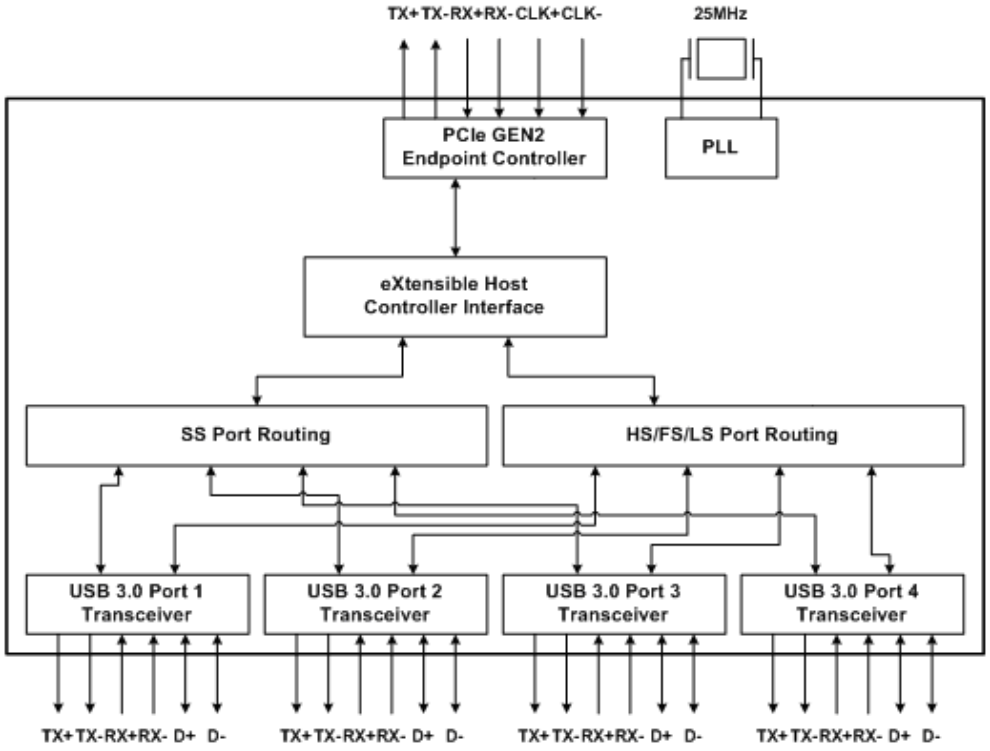


Figure 1 – VL805 Block Diagram

3. VL805 Pin Diagram

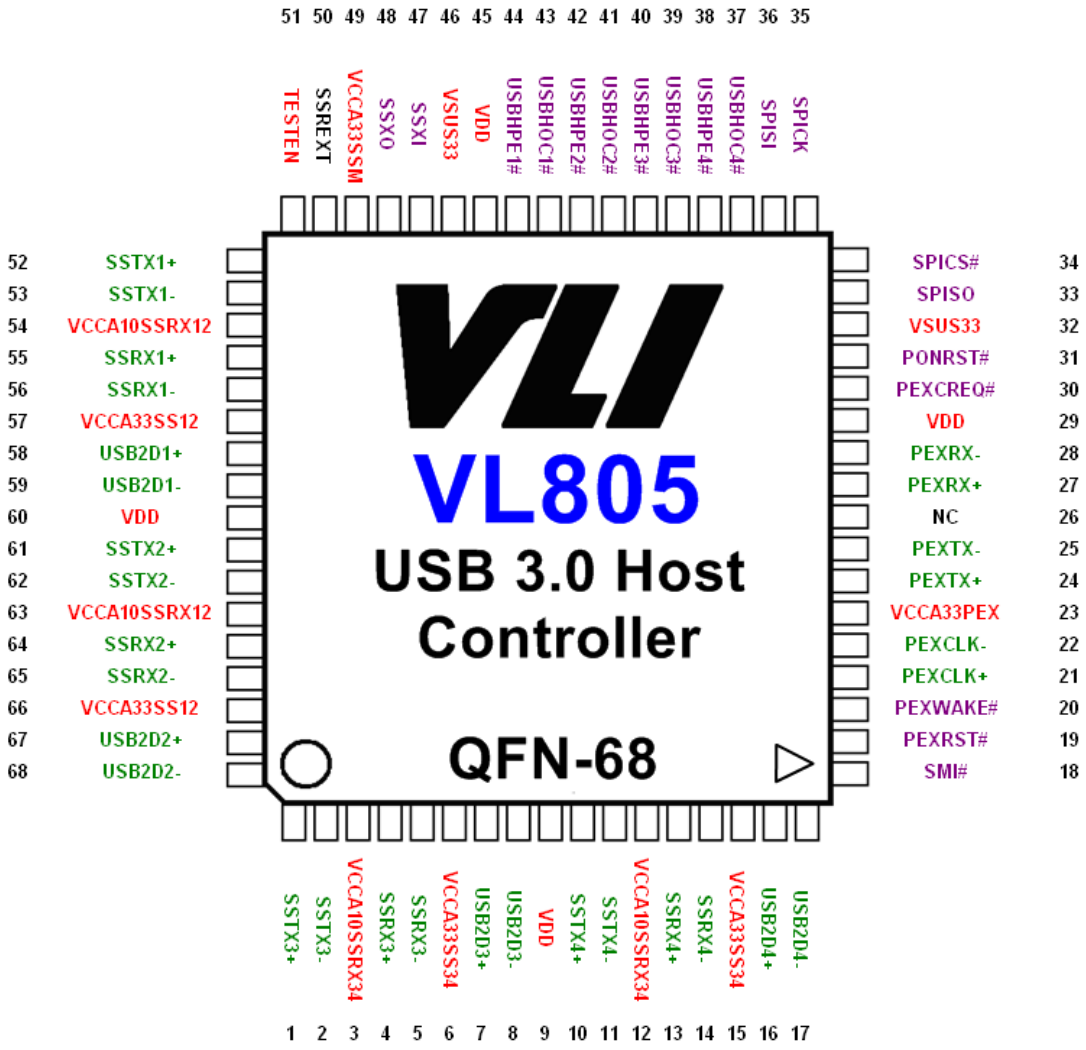


Figure 2 – VL805 Pin Diagram

4. PIN Function

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Open drain	OD	Allows multiple devices to share as a wire-OR.
Analog differential	A_{DIFF}	Signal pair for the twisted-pair interface
Analog bias or reference signal	A_{BIAS}	Must be tie to external resistor, as shown in the system schematic.
Power	PWR	A power pin
Ground	GND	A ground pin

Power and Ground

Pin Name	Pin #	I/O	Signal Description
VDD	9,29,45,60	PWR	1.05V Core power
VSUS33	32,46	PWR	3.3V suspend power

PCI Express x1 Interface

Pin Name	Pin #	I/O	Signal Description
VCCA33PEX	23	PWR	PCIE PHY 3.3V
PEXTX0+	24	A_{DIFF}	PCIE Differential Transmit Data +
PEXTX0-	25	A_{DIFF}	PCIE Differential Transmit Data -
PEXRX0+	27	A_{DIFF}	PCIE Differential Receive Data +
PEXRX0-	28	A_{DIFF}	PCIE Differential Receive Data -
PEXCLK+	21	A_{DIFF}	PCIE Differential Reference Clock +/-. The PCIE externally provided differential clock with 100MHz. The SSC (Spread Spectrum Clock) is allowed and recommended within +300ppm and – 2300ppm.
PEXCLK-	22	A_{DIFF}	

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	47	I	25M crystal input, it can alternately be driven by external clock source (**1.05V voltage swing main power source**) with SSXO unconnected.
SSXO	48	O	25M crystal output
SSREXT	50	A_{BIAS}	Connect to Band Gap reference resistor to add an external 6.04K(1%)resistor between this pin and ground for SuperSpeed USB

SPI Flash Interface

Pin Name	Pin #	I/O	Signal Description
SPICS#	34	O	SPI Chip Select
SPISCLK	35	O	SPI Serial Clock Input
SPISI	36	O	SPI Serial Data Input
SPISO	33	I	SPI Serial Data Output

USB 3.0 Root Hub Interface

Pin Name	Pin #	I/O	Signal Description
SSTX1+	52	A_{DIFF}	USB 3.0 DP1 Port Differential Transmit Data +
SSTX1-	53	A_{DIFF}	USB 3.0 DP1 Port Differential Transmit Data -
SSRX1+	55	A_{DIFF}	USB 3.0 DP1 Port Differential Receive Data +
SSRX1-	56	A_{DIFF}	USB 3.0 DP1 Port Differential Receive Data -
VCCA10SSRX12	54,63	PWR	USB PHY 1.05V
VCCA33SS12	57,66	PWR	USB PHY 3.3V suspend power
SSTX2+	61	A_{DIFF}	USB 3.0 DP2 Port Differential Transmit Data +
SSTX2-	62	A_{DIFF}	USB 3.0 DP2 Port Differential Transmit Data -
SSRX2+	64	A_{DIFF}	USB 3.0 DP2 Port Differential Receive Data +
SSRX2-	65	A_{DIFF}	USB 3.0 DP2 Port Differential Receive Data -
SSTX3+	1	A_{DIFF}	USB 3.0 DP3 Port Differential Transmit Data +
SSTX3-	2	A_{DIFF}	USB 3.0 DP3 Port Differential Transmit Data -
SSRX3+	4	A_{DIFF}	USB 3.0 DP3 Port Differential Receive Data +
SSRX3-	5	A_{DIFF}	USB 3.0 DP3 Port Differential Receive Data -
VCCA10SSRX34	3,12	PWR	USB PHY 1.05V
VCCA33SS34	6,15	PWR	USB PHY 3.3V suspend power
SSTX4+	10	A_{DIFF}	USB 3.0 DP4 Port Differential Transmit Data +
SSTX4-	11	A_{DIFF}	USB 3.0 DP4 Port Differential Transmit Data -
SSRX4+	13	A_{DIFF}	USB 3.0 DP4 Port Differential Receive Data +
SSRX4-	14	A_{DIFF}	USB 3.0 DP4 Port Differential Receive Data -
VCCA33SSM	49	PWR	USB 3.3V suspend power for PLL

USB 2.0 Root Hub Interface

Pin Name	Pin #	I/O	Signal Description
USB2D1+	58	A_{DIFF}	USB 2.0 DP1 Bus Data Plus (D+)
USB2D1-	59	A_{DIFF}	USB 2.0 DP1 Bus Data Minus (D–)
USB2D2+	67	A_{DIFF}	USB 2.0 DP2 Bus Data Plus (D+)
USB2D2-	68	A_{DIFF}	USB 2.0 DP2 Bus Data Minus (D–)
USB2D3+	7	A_{DIFF}	USB 2.0 DP3 Bus Data Plus (D+)
USB2D3-	8	A_{DIFF}	USB 2.0 DP3 Bus Data Minus (D–)
USB2D4+	16	A_{DIFF}	USB 2.0 DP4 Bus Data Plus (D+)
USB2D4-	17	A_{DIFF}	USB 2.0 DP4 Bus Data Minus (D–)

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	51	I	Test Mode Enable Do not connect for normal operation. Internal pull down.
Reserved	26		

Side Band signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBHPE1#	44	OD	DP1 Power Enable
USBHPE2#	42	OD	DP2 Power Enable
USBHPE3#	40	OD	DP3 Power Enable
USBHPE4#	38	OD	DP4 Power Enable
USBHOC1#	43	I	DP1 Over Current Indicator
USBHOC2#	41	I	DP2 Over Current Indicator
USBHOC3#	39	I	DP3 Over Current Indicator
USBHOC4#	37	I	DP4 Over Current Indicator
PONRST#	31	I	Power on reset signal.
PEXCREQ#	30	O	PCIE Express "CLKREQ#"Signal. Request to run/stop reference clock.
PEXRST#	19	I	System reset. **PCI Express Reset**. When PEXRST# is asserted low, the chip performs an internal system Hardware reset.
SMI#	18	OD	System Management Interrupt. To support USB function with BIOS, need to connect this pin to the platform chipset. If not to support USB function with BIOS, just pull up to 3.3V with 10K resistor.
PEXWAKE#	20	OD	Link Reactivation. **System Wake up**. The Signal is asserted low to reactivate the PCI Express slot's main power rails and reference clocks.

5. Electrical Characteristics

5.1 Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Unit
VCCA10	Analog 1.05V power supply	1.0	1.05	1.1	V
VCCA33	Analog 3.3V power supply	3.0	3.3	3.6	V
VDD	Digital core power supply	1.0	1.05	1.1	V
VSUS33	Aux Power 3.3 power supply	3.0	3.3	3.6	V
PEXRST# V_{IH}	PCIE Reset Input High Voltage	2.0	3.3	3.6	V
PEXRST# V_{IL}	PCIE Reset Input Low Voltage	-0.5	0	0.8	V
T_A	Operating ambient temperature	0		70	℃

5.2 Absolute Maximum Rating

Symbol	Parameters	Rating	Units
VCCA10	Analog 1.05V power supply	-0.5 to +1.4	V
VCCA33	Analog 3.3V power supply	-0.5 to +4.6	V
VDD	Digital core power supply	-0.5 to +1.4	V
VSUS33	Aux Power 3.3 power supply	-0.5 to +4.6	V

5.3 PCI Express Reference Clock

Symbol	Parameters	Min.	Max.	Units
T_{RISE}	Rising Edge Rate	0.6	4.0	V/ns
T_{FALL}	Falling Edge Rate	0.6	4.0	V/ns
V_{IH}	Differential Input High Voltage	+150		mV
V_{IL}	Differential Input Low Voltage		-150	mV
V_{cross}	Absolute crossing point voltage	+250	+550	mV
$V_{CROSS\ DELTA}$	Variation of VCROSS over all rising clock edgw		+140	mV
V_{RB}	Ring-back Voltage Margin	-100	+100	mV
T_{STABLE}	Time before V_{RB} is allowed	500		ps
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm
$T_{PERIOD\ ABS}$	Absolute Period(including jitter and Spread Spectrum)	9.847	10.203	ns
$V_{CCJITTER}$	Cycle to Cycle Jitter		150	ps

V_{MAX}	Absoulte Max input voltage		+1.15	V
V_{MIN}	Absoulte Min input voltage		-0.3	V
Z_{C-DC}	Clock source DC impedance	40	60	Ω
	Duty Cycle	40	60	%
	Rising edge rate to falling dege rate matcing		20	%

5.4 USB Interface

Symbol	Parameters	Min.	Max.	Units
	Output pin impedance	40.5	49.5	Ω
Input Levels for Low/Full Speed				
V_{IH}	High-level input voltage(drive)	2.0		V
V_{IHZ}	High-level input voltage(floating)	2.7	3.6	V
V_{IL}	Low-level input voltage		0.8	V
V_{DI}	Differential input sensitivity	0.2		V
V_{CM}	Differential input common mode range	0.8	2.5	V
Output Levels for Low/Full Speed				
V_{OH}	High-level output voltage	2.8	3.6	V
V_{OL}	Low-level output voltage	0.0	0.3	V
V_{OSE1}	SE1	0.8		V
V_{CRS}	Output signal crossover point voltage	1.3	2.0	V
Input Levels for High-Speed				
V_{HSSQ}	High-speed squelch detection threshold (differential signal)	100	150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal)	525	625	mV
V_{HSCM}	High-speed data signaling common mode voltage range	-50	+500	mV
Output Levels for High Speed				
V_{HSOI}	High-speed idle state	-10	+10	mV
V_{HSOH}	High-speed data signaling High	360	440	mV

V_{HSOL}	High-speed data signaling Low	-10	+10	mV
V_{CHIRPJ}	Chrip J level(differential signal)	700	1100	mV
V_{CHIRPK}	Chrip K level(differential signal)	-900	-500	mV

6. PCI Configuration Registers

Header Registers (00-3Fh)

Offset Address: 01-00h
Vendor ID Default Value: 1106h

Bit	Attribute	Default	Description	Mnemonic
15:0	RO	1106h	VIA Technology ID Code	**VID**

Offset Address: 03-02h
Device ID Default Value: 3483h

Bit	Attribute	Default	Description	Mnemonic
15:0	RO	3483h	Device ID Code	**DEVID**

Offset Address: 05-04h (D18F0)
PCI Command Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:11	RO	0	Reserved	**RESERVED**
10	RW	0	Interrupt Disable	**INTRDIS**
9	RO	0	Reserved	**RESERVED**
8	RW	0	SERR Enable	**SERREN**
7	RO	0	Reserved	**RESERVED**
6	RW	0	Parity Error Response	**RPTYERR**
5	RO	0	Reserved	**RESERVED**
4	RO	0	Memory Write and Invalidate	**MWRMEN**
3	RO	0	Reserved **Special cycle monitoring.** **Fixed at 0b (Not supported).**	**RESERVED**
2	RW	0	Bus Master	**BMASTREN**
1	RW	0	Memory Space	**MMSPACE**
0	RW	0	I/O Space	**IOSPACE**

Offset Address: 07-06h
PCI Status Default Value: 0010h

Bit	Attribute	Default	Description	Mnemonic
15	RW1C	0	Detected Parity Error	**DPRTYERR**
14	RW1C	0	Signaled System Error	**SSYSERR**
13	RW1C	0	Received Master Abort (Except Special Cycle) **0: No abort received** **1: Transaction aborted by the Master**	**TMABORTS**
12	RW1C	0	Received Target Abort **0: No abort received** **1: Transaction aborted by the Target**	**TTABORTR**
11	RW1C	0	Signaled Target Abort	**STABORT**
10:9	RO	0	DEVSEL# Timing **Fixed at 01b.** **00: Fast** **01: Medium** **10: Slow** **11: Reserved**	**DEVSELTM**
8	RW1C	0	Master Data Parity Error	**MDPRTYERR**
7:4	RO	01h	Fixed at 01h (for PCI PMI)	**RESERVED**
3	RO	0	Interrupt Status	**INTRSTS**
2:0	RO	0	Reserved	**RESERVED**

Offset Address: 08h
Revision ID Default Value: 01h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	00h	Revision ID	**REVID**

Offset Address: 0B-09h (D18F0)
Class Code Default Value: 0C0330h

Bit	Attribute	Default	Description	Mnemonic
23:0	RO	0C0330h	Class Code for USB3.0 XHCI Host Controller	**CLSCODE**

Offset Address: 0Ch
Cache Line Size Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	0	Cache Line Size	**CACHLINE**

Offset Address: 0Dh
Latency Timer Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	0	Latency Timer	**LATTM**

Offset Address: 0Eh
Header Type Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	00h	Header Type	**HDTYPE**

Offset Address: 0Fh
Built In Self Test (BIST) Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	0	BIST **Fixed at 00h**	**BIST**

Offset Address: 13-10h
XHCI Memory Mapped I/O Low Base Address Default Value: 00000004h

Bit	Attribute	Default	Description	Mnemonic
31:12	RW	0	XHCI Memory Mapped I/O Registers Low Base Address **Memory Address for the base of the USB 3.0 XHCI MMIO Register..**	**BASEADDR0_LO**
11:3	RO	0	Reserved	**RESERVED**
2:1	RO	10b	Base Address Type **Reads 10b for 64-bit addressing.**	**BARTYPE0**
0	RO	0	Reserved	**RESERVED**

Offset Address: 17-14h (D18F0)
XHCI Memory Mapped I/O High Base Address Default Value: 00000000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	XHCI Memory Mapped I/O Registers High Base Address **Memory Address for the base of the USB 3.0 XHCI MMIO Register..**	**BASEADDR0_HI**

Offset Address: 18-2Bh (D18F0) – Reserved

Offset Address: 2D-2Ch (D18F0)
Subsystem Vendor ID Default Value: 1106h

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	1106h	Subsystem Vendor ID	**SYSVID**

Offset Address: 2F-2Eh
Subsystem ID Default Value: 3483h

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	3483h	Subsystem ID	**SUBSID**

Offset Address: 30-33h Reserved

Offset Address: 34h
Capability Pointer Default Value: 80h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	80h	Capability Pointer **This register contains the offset address from the start of the configuration space.** **Fixed at 80h.**	**CAPPTR**

Offset Address: 35-3Bh Reserved

Offset Address: 3Ch
Interrupt Line Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	0	USB Interrupt Routing **'h00: Disable** **'h01: IRQ1** **'h02: Reserved** **'h03: IRQ3** **'h04: IRQ4** **'h05: IRQ5** **'h06: IRQ6** **'h07: IRQ7** **'h08: IRQ8** **'h09: IRQ9** **'h0a: IRQ10** **'h0b: IRQ11** **'h0c: IRQ12** **'h0d: IRQ13** **'h0e: IRQ14** **Other: Disable**	**INTLN**

Offset Address: 3Dh
Interrupt Pin Default Value: 01h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	01h	Interrupt Pin **Fixed at 01h (INTA#).**	**INTPIN**

Offset Address: 3E-3Fh Reserved

XHCI-Specific Configuration Registers (40-FFh)

Offset Address: 40-43h Reserved

Offset Address: 48-4Bh
XHCI CRCR Mirror Low Register Default Value: 00000000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	XHCI CRCR Mirror Low Register	**CRCR_MIRROR_LO**

Offset Address: 4C-4Fh Reserved

Offset Address: 50-53h
XHCI MCU Firmware Version Default Value: 00000000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	XHCI MCU Firmware Version	**FW_VERSION**

Offset Address: 5C-5Dh
Subsystem Vendor ID For SW Default Value: 1106h

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	1106h	Subsystem Vendor ID (SW can update)	**SYSVID_SW**

Offset Address: 5E-5Fh
Subsystem ID For SW Default Value:3483h

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	3483h	Subsystem ID (SW can update)	**SUBSID_SW**

Offset Address: 60h
Serial Bus Release Number (SBRN) Default Value: 30h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	30h	Serial Bus Specification Release Number. **All other combinations are reserved.** **Bits[7:0] Release Number** **30h Release 3.0**	**SBRN**

Offset Address: 61h
Frame Length Adjustment (FLADJ) Default Value: 20h

Bit	Attribute	Default	Description	Mnemonic
7:6	ROS	0	Reserved	**RESERVED**
5:0	RWS	20h	Frame Length Timing Value. **Each decimal value change to this register corresponds to 16** **high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a** **SOF microframe length) is equal to 59488 + value in this field. The default value is decimal 32** **(20h), which gives a SOF cycle time of 60000.** **Frame Length** **(# HS bit times) FLADJ Value** **(decimal) (decimal)** **59488 0 (00h)** **59504 1 (01h)** **59520 2 (02h** **…** **59984 31 (1Fh)** **6000032 (20h)** **…** **60480 62 (3Eh)** **60496 63 (3Fh)**	**FLADJ**

Offset Address: 78-7Bh
XHCI Optional Bits Configuration Address Default Value: 00000000h

Bit	Attribute	Default	Description	Mnemonic
31:20	RO	0	Reserved	**RESERVED**
19:0	RW	0	XHCI Option Bits Configuration Address.	**OPTCFGADDR**

Offset Address: 7C-7Fh
XHCI Optional Bits Configuration Data Default Value: 00000000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	XHCI Option Bits Configuration Data.	**OPTCFGDATA**

Offset Address: 80h
Power Management Capability ID Default Value: 01h

Bit	Attribute	Default	Description	Mnemonic
7:0	ROS	01h	Power Management Capability ID	**PMCAPID**

Offset Address: 81h
Next Item Pointer 1 Default Value:90h

Bit	Attribute	Default	Description	Mnemonic
7:0	ROS	90h	Next Item Pointer 1	**PMNXTPTR**

Offset Address: 82-83h
Power Management Capability Default Value:4803h

Bit	Attribute	Default	Description	Mnemonic
15:0	ROS	4803h	Power Management Capability	**PMCAP**

Offset Address: 84-85h
Power Management Capability Control / Status Default Value:0000h

Bit	Attribute	Default	Description	Mnemonic
15	RWS	0	PME Status **0: Not active** **1: Active**	**PMESTATUS**
14:9	ROS	0	Reserved	**RESERVED**
8	RWS	0	PME Enable **0: Disable** **1: Enable**	**PMEEN**
7:2	ROS	0	Reserved	**RESERVED**
1:0	RWS	00b	Power State **00: D0** **01: D1** **10: D2** **11: D3 Hot**	**PMSTATE**

Offset Address: 86-8Fh

Offset Address: 90h
MSI Capability ID Default Value:05h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	05h	MSI Capability ID	**MSIID**

Offset Address: 91h
Next Item Pointer 2 Default Value:C4h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	C4h	Next Item Pointer 2	**MSINXTPTR**

Offset Address: 92-93h
MSI Message Control Default Value:0084h

Bit	Attribute	Default	Description	Mnemonic
15:9	RO	0	Reserved	**RESERVED**
8	RO	0	Per-vector Masking Capable **1: Function supports MSI per-vector masking** **0: Function does NOT support MSI per-vector masking**	**MSIMSKCAP**
7	RO	1b	64 Bit Address Capable **1: Function is capable of sending a 64-bit message address.** **0: Function is NOT capable of sending a 64-bit message address.**	**MSIADDR64CAP**
6:4	RW	0	Multiple Message Enable **Software writes to this field to indicate the number of allocated vectors. The number of allocated vectors is aligned to a power of two.** **000: 1 vector allocated** **001: 2 vectors allocated** **010: 4 vectors allocated** **011: 8 vectors allocated** **100: 16 vectors allocated** **101: 32 vectors allocated** **110: Reserved** **110: Reserved**	**MSIMLTEN**
3:1	RO	010b	Multiple Message Capable **System software reads this field to determine the number of requested vectors.** **000: 1 vector allocated** **001: 2 vectors allocated** **010: 4 vectors allocated** **011: 8 vectors allocated** **100: 16 vectors allocated** **101: 32 vectors allocated** **110: Reserved** **110: Reserved**	**MSIMULCAP**
0	RW	0	MSI Enable **If 1 and the MSI-X Enable in MSI-X Message Control register is 0, the function is permitted to use MSI to request service and is prohibited from using its INTx pin.** **If 0, the function is prohibited from using MSI to request service.**	**MSIEN**

Offset Address: 94-97h
MSI Message Address Low Default Value: 00000000h

Bit	Attribute	Default	Description	Mnemonic
31:2	RW	0	Message Address (Low 32 Bits). **System specified message address.**	**MSIADDRLO**
1:0	RO	0	Reserved	**RESERVED**

Offset Address: 98-9Bh
MSI Message Address High Default Value: 00000000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	Message Address (High 32 Bits). **System specified message address.**	**MSIADDRHI**

Offset Address: 9C-9Dh
MSI Data Default Value:0000h

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	0	Message Data. **System specified message data.**	**MSIDATA**

Offset Address: 9E-FFh Reserved

7. Host Controller Capability Registers

Host Controller Capability Registers(Base+00h-Base+1Bh)

Note:The beginning of the host controller’s MMIO address space is referred to as Base Address Register at Rx10h of PCI Configuration Space throughout this document.

Offset Address: 00h (USB3.0-MMIO)
Capability Registers Length (CAPLENGTH) Default Value: 20h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	20h	Capability Registers Length **This register is used as an offset to add to register base to find the beginning of the Operational Register Space.**	**CAPLENGTH**

Offset Address: 01h (USB3.0-MMIO) – Reserved

Offset Address: 03-02h (USB3.0－MMIO)
Host Controller Interface Version Number (HCIVERSION) Default Value: 0100h

Bit	Attribute	Default	Description	Mnemonic
15:0	RO	0100h	Host Controller Interface Version Number **This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0.**	**HCIVERSION**

Offset Address: 07-04h (USB3.0－MMIO)
Structural Parameters 1 (HCSPARAMS1) Default Value: 05000420h

Bit	Attribute	Default	Description	Mnemonic
31:24	RO	05h	Number of Ports (MaxPorts). **This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space (see Table 26). Valid values are in the range of 1h to FFh.**	**MAXPORTS**
23:19	RO	0	Reserved	**RESERVED**
18:8	RO	04h	Number of Interrupters (MaxIntrs). **This field specifies the number of Interrupters implemented on this host controller. Each Interrupter is allocated to a vector of MSI-X and controls its generation and moderation.** **The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space (see section 5.5). Valid values are in the range of 1h to 400h. A ‘0’ in this field is undefined.**	**MAXINTRS**
7:0	RO	20h	Number of Device Slots (MaxSlots). **This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of ‘0’ is reserved.**	**MAXSLOTS**

Offset Address: 0B-08h (USB3.0－MMIO)

Structural Parameters 2 (HCSPARAMS2) **Default Value: FC000031h**

Bit	Attribute	Default	Description	Mnemonic
31:27	RO	1Fh	Max Scratchpad Buffers (Max Scratchpad Bufs). **Valid values are 0-31. This field indicates the number of Scratchpad Buffers system software shall reserve for the xHC. See section 4.20 for more information.**	**MAXSCRBUF**
26	RO	1b	Scratchpad Restore (SPR). **If *Max Scratchpad Buffers* is > '0' then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If *Max Scratchpad Buffers* is = '0' then this flag shall be '0'. See section 4.23.2 for more information. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events.**	**SPR**
25:21	RO	0	Max Scratchpad Buffers (Max Scratchpad Bufs Hi)	**MAXSCRBUF_HI**
20:8	RO	0	Reserved	**RESERVED**
7:4	RO	3h	Event Ring Segment Table Max (ERST Max). **Valid values are 0 – 15. This field determines the maximum value supported the *Event Ring Segment Table Base Size* registers (5.5.2.3.1), where: The maximum number of Event Ring Segment Table entries = 2 ERST Max. e.g. if the ERST Max = 7, then the xHC *Event Ring Segment Table(s)* supports up to 128 entries, 15 then 32K entries, etc.**	**MAXERST**
3:0	RO	1h	Isochronous Scheduling Threshold (IST). **The value in this field indicates to system software the minimum distance (in time) that it must stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/microframes. If bit [3] of IST is set to '0', software can add a TRB no later than IST[2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed. Refer to Section 4.14.2 for details on how software uses this information for scheduling isochronous transfers.**	**IST**

Offset Address: 0F-0Ch (USB3.0－MMIO)

Structural Parameters 3 (HCSPARAMS3) **Default Value: 00E70004h**

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	00E7h	U2 Device Exit Latency. **Worst case latency to transition from U2 to U0. Applies to all root hub ports.** **The following are permissible values:** **Value Description** **0000h zero** **0001h less than 1 μs.** **0002h less than 2 μs.** **…** **07FFh less than 2047 μs.** **0800-FFFFh reserved**	**U2DEVEXTLT**
15:8	RO	0	Reserved	**RESERVED**
7:0	RO	04h	U1 Device Exit Latency. **Worst case latency to transition a root hub port link state from U1 to U0. Applies to all root hub ports.** **The following are permissible values:** **Value Description** **00h zero** **01h less than 1 μs** **02h less than 2 μs.** **…** **0Ah less than 10 μs.** **0B-FFh reserved**	**U1DEVEXTLT**

Offset Address: 13-10h (USB3.0－MMIO)

Capability Parameters (HCCPARAMS) **Default Value: 002841EBh**

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	0028h	xHCI Extended Capabilities Pointer (xECP). **This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability.** **For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculated the following effective address of the first extended capability: 1000h + (0068h << 2) -> 1000h + 01A0h -> 11A0h**	**XECP**
15:12	RO	4h	Maximum Primary Stream Array Size (MaxPSASize). **This fields identifies the maximum size Primary Stream Array that the Xhc supports. The *Primary Stream Array* size = 2*MaxPSASize*+1. Valid *MaxPSASize* values are 1 to 15.**	**MAXPSASIZE**
11:9	RO	0	Reserved	**RESERVED**
8	RO	1b	Parse All Event Data (PAE)	**PAE**
7	RO	1b	No Secondary SID Support (NSS). **This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1' in this bit indicates that Secondary Stream ID decoding is not supported. A '0' in this bit indicates that Secondary Stream ID decoding is supported. (refer to Sections 4.12.2 and 6.2.3).**	**NSS**

6	RO	1b	Latency Tolerance Messaging Capability (LTC). **This field indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A '1' in this bit indicates that LTM is supported. A zero in this bit indicates that LTM is not supported. See section 4.13.1 for more information on LTM.**	**LTC**
5	RO	1b	Light HC Reset Capability (LHRC). **This field indicates whether the host controller implementation supports a Light Host Controller Reset. A '1' in this bit indicates that Light Host Controller Reset is supported. A '0' in this bit indicates that Light Host Controller Reset is not supported. The value of this field affects the functionality of the Light Host Controller Reset field in the USBCMD register (see Section 5.4.1).**	**LHRC**
4	RO	0	Port Indicators (PIND). **This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator. See Section 5.4.8 for definition of the *Port Indicator Control* field.**	**PIND**
3	RO	1b	Port Power Control (PPC). **This field indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches. The value of this field affects the functionality of the *Port Power* field in each port status and control register (see Section 5.4.8).**	**PPC**
2	RO	0	Context Size (CSZ). **If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is set to '0', then the xHC uses 32 byte Context data structures. Note: This flag does *not* apply to Stream Contexts.**	**CSZ**
1	RO	1b	BW Negotiation Capability (BNC). **This field identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this field have the following interpretation: 0b BW Negotiation not implemented_ 1b BW Negotiation implemented See section 4.16 for more information on Bandwidth Negotiation.**	**BNC**
0	RO	1b	64-bit Addressing Capabilitya (AC64). **This field documents the addressing range capability of this implementation. The value of this field determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this field have the following interpretation: 0b 32-bit address memory pointers implemented_ 1b 64-bit address memory pointers implemented If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.**	**AC64**

Offset Address: 17-14h (USB3.0－MMIO)

Doorbell Offset (DBOFF) Default Value:00000100h

Bit	Attribute	Default	Description	Mnemonic

31:2	RO	40h	Doorbell Array Offset. **This field defines the Dword offset of the Doorbell Array base address from the Base (i.e. the base address of the xHCI Capability register address space).**	**DBOFF**
1:0	RO	0	Reserved	**RESERVED**

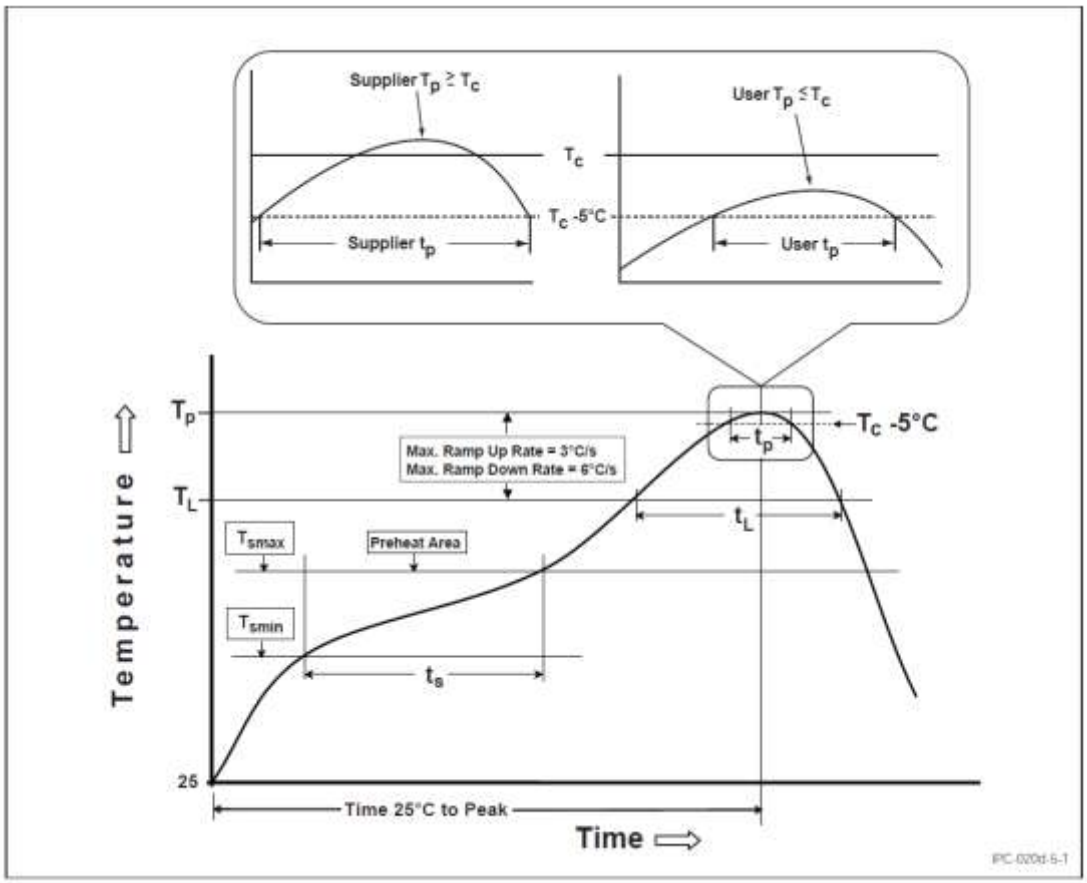
Offset Address: 1B-18h (USB3.0－MMIO)

Runtime Register Space Offset (RTSOFF) **Default Value: 00000200h**

Bit	Attribute	Default	Description	Mnemonic
31:5	RO	10h	Runtime Register Space Offset. **This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. i.e. Runtime Register Base Address = Base + Runtime Register Set Offset.**	**RTSOFF**
4:0	RO	0	Reserved	**RESERVED**

Offset Address: 1C-1Fh (USB3.0-MMIO) – Reserved

8. General Reflow Profile Guidelines



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p **shall** be within ± 2 °C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.

For example, if T_c is 260 °C and time t_p is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

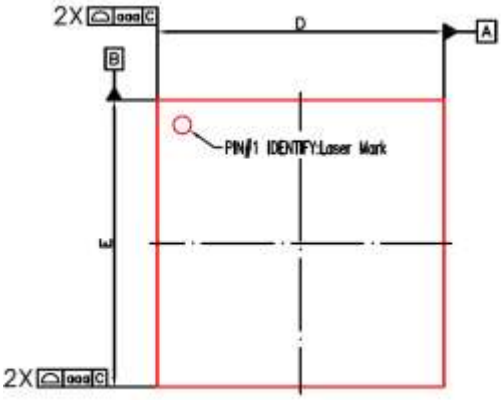
Note 3: All components in the test load **shall** meet the classification profile requirements.

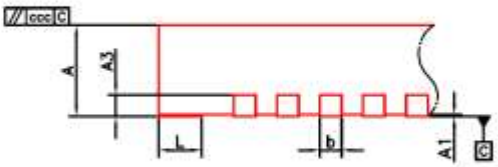
Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

9. Package Mechanical Specifications

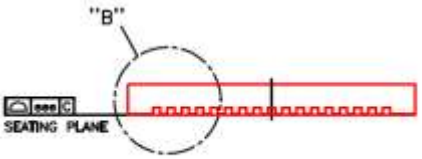
Pb-free Maximum Temperature for IR Reflow

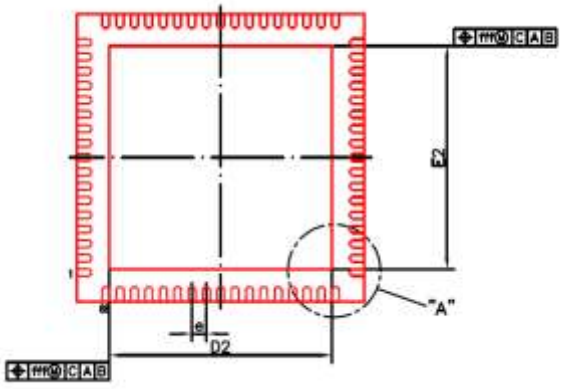
Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds

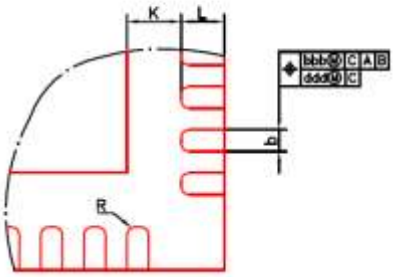




DETAIL : "B"







DETAIL : "A"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.05	6.20	6.35	0.238	0.244	0.250
E2	6.05	6.20	6.35	0.238	0.244	0.250
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 3 – Mechanical Specification – QFN68 8x8 mm Package

10. Package Top Side Marking

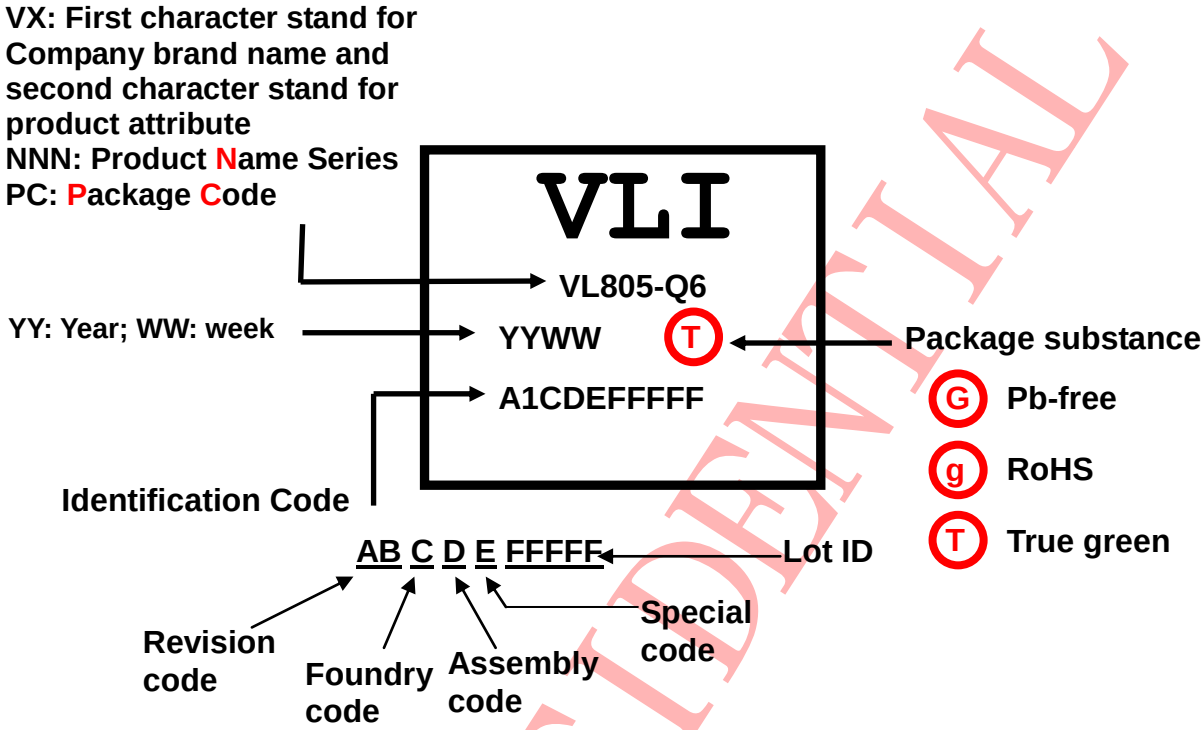


Figure 4 – Package Top Side Marking

11. Order Information

Part Number	Package Type
VL805 – Q6 T	QFN68 8x8 mm

VIA Labs, Inc.

www.via-labs.com

7F, 529-1, Zhongzheng Rd.,

Xindian District, New Taipei City 231 Taiwan

Tel: (886-2) 2218-1838

Fax: (886-2) 2218-8924

Email: sales@via-labs.com.tw